Amendments to the Claims:

This listing of Claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A processor architecture adapted to program languages operating with a sequential flow of instructions and handling data through use of simple values and lists and dynamically allocated arrays, and ~~comprising an~~ comprising:

instruction holding means for holding instructions; ~~, a~~

data memory means for storing data objects; ~~, and~~

execution means for executing an instruction; ~~, characterized by~~

means for storing and handling argument values comprising simple values and references to data objects in dependence of an actual instruction from the instruction holding ~~means~~ means, said dependence being called a binding; ~~,~~

wherein said binding substituting a parameter reference in an actual instruction with an argument value and providing the actual instruction and the actual argument value to the execution means for executing said instruction;

wherein said means for storing and handling is separate from said execution means and said instruction holding means; and

means to increment reference counts to a data object and to decrement reference counts to a data object in dependence of an actual instruction from the instruction holding means, and in dependence of the means, which handles simple values and references, storing a reference to said data object.

2. (Currently Amended) A processor architecture according to claim 1, ~~characterized by~~ comprising means for handling storage of simple data and references to data objects in the means, said stored data and references to data objects being referred to, by means of identifiers, from instructions from the instruction holding means;

storage means in the means for handling storage of simple data and references to data objects.

3. (Currently Amended) A processor architecture according to claim 1, ~~characterized in that~~ wherein the means for handling the storage of values comprises a parameter memory means having means for keeping notice of the bindings to the stored values, and having storage means for storing said values.

4. –5. (Cancelled)

6. (Currently Amended) A processor architecture according to claim 3, ~~characterized in that~~ wherein in the parameter memory for storing and managing scope information for the stored parameters, where the scope information determines which parameters are currently valid and eligible to be read out from the storage.

7. (Currently Amended) A processor architecture according to claim 3, ~~characterized in that~~ wherein in the parameter memory for storing and managing information for scope and values, where the means is used for storing and managing information for scope and data values, where the process information determines which scopes and values are currently valid and eligible to be read out from the storage.

8. (Currently Amended) A processor architecture according to claim 3, ~~characterized by~~ comprising a process identification register for identification of the currently executed process; a scope identification register for identification of the currently valid scope.

9. (Currently Amended) A processor architecture according to claim 3, ~~characterized in that~~ wherein at least ~~the~~ a top of at least one priority queue of processes to be executed is kept available for reading, wherein each process

corresponds to a process descriptor, and wherein and that at least part of the process descriptor of ~~the~~ a next process to be executed process is kept available for reading.

10. (Currently Amended) A processor architecture according to claims 9, ~~characterized in that~~ wherein in order to make a process switch the means for handling values and references:

creates a new scope and at least the program counter is stored in the parameter memory using the new scope;

stores said new scope value in the process descriptor of the current process, said process descriptor may be stored in the data memory;

restores the scope value for the process switch from the process descriptor of said process;

sets the process switch to be the current process; and

reads at least the program counter from the parameter memory and performs the restoring.

11. (Currently Amended) A processor architecture according to claim 1, ~~characterized by~~ comprising instructions having only one instruction format, where each instruction is composed of a distinct number of sub-instructions, each of which has in turn the same and only one format comprising a first part and a second part, the first part determining the action to take and the second part providing a value to use in the action.

12. (Currently Amended) A processor architecture according to claim 1, adapted to execution of languages using functions and dynamic memory allocation ~~characterized by~~ comprising a set of instructions comprising dedicated instructions for making function calls, function returns, and parameter transfer between functions.

13. (Currently Amended) A processor architecture according to claim 11, ~~characterized by~~ comprising a set of instructions comprising dedicated instructions for

incrementing and decrementing the number of references to data objects stored in the data memory.

14. (Currently Amended) A processor architecture according to claim 1, ~~characterized in that~~ wherein it is adapted to process parts of computer programs written in a functional language.